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EXAMINER	
QI, ZHI QIANG	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/550,282	PARK ET AL.	
	Examiner	Art Unit	
	Mike Qi	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6,11-15,17 and 19-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,11-15,17 and 19-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 15 is objected to because of the following informalities:

Regarding claim 15, recitation ". . . forming a gate line and a gate electrode of a thin film transistor to be connected with the gate line on a transparent substrate; forming an insulating layer electrically insulating said gate line and the gate electrode;. . ." in which the gate electrode is connected with the gate line, so that an insulating layer electrically insulating the gate line and the gate electrode is not correct. The gate line is used for applying scanning signal to the gate electrode, so that the gate electrode is not insulated from the gate line. The limitation of "forming an insulating layer . . ." should be after the limitation of "forming a data line. . .". Such that the limitation should be ". . . forming an insulating layer electrically insulating said gate line and the gate electrode from the data line; . . .". The claim 22 describes forming a gate line and gate electrode connected thereto on a transparent substrate and forming an insulating layer over the gate line and gate electrode, such that the gate line and gate electrode are connected and there are no insulation between the gate line and the gate electrode.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 11, 14-15, 22 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,259,200 (Morita et al).

Regarding claims 1, 15 and 22, Morita discloses (col.5, lines 59 – col.6, line 65; Figs.5-6) that a liquid crystal display device comprising:

- gate line (43) formed on a transparent substrate (1), and gate electrode (G) of the TFT (3) to be connected with the gate line (43) on the transparent substrate (1);
- data lines (signal line 10) crossing the gate line (43) and formed on the transparent substrate (1); and the data line (10), source electrode and drain electrode over the transparent substrate (1), the source electrode and the drain electrode being respectively disposed in source area (7) and drain area (8), and the source electrode being connected with the data line (10) through contact hole (S);
- gate insulating layer (4a,4b) electrically insulating the data line (43) from the gate line (10) and gate electrode (G); and over the gate line (43) and the gate electrode (G);
- semiconductor layer (2) over the gate electrode (G);
- thin film transistor (TFT) (3) formed at an intersection of the gate line (43) and the data line (10), and connected to the gate line (43) and the data line (10), and the TFT being disposed in an area having a channel area (between the source area and the drain area), a source area (7) (first

portion of the semiconductor layer 2) and a drain area (8) (second portion of the semiconductor layer 2); and the TFT (3) having gate electrode, source electrode and drain electrode;

- passivation layer (planarization film 12 functions as passivation layer (col.4, lines 31-32) formed over the TFT (3); and having contact hole exposing the drain electrode over the transparent substrate (1);
- pixel electrode (14) having portions formed on the surface of the passivation layer(planarization film 12 functions as a passivation layer), but not over the TFT (3); and to the drain electrode via the contact hole.

Morita does not expressly discloses in the Figs.4-6 that:

1) a low reflective layer covers at least a portion of the gate line or a portion of the data line or formed on (to shield) the first portion (source area);

2) the second portion (drain area); and no black layer or light shielding layer between the pixel electrode and the upper substrate and above the low reflective layer.

However, Morita discloses (col.4, lines 51-67; Fig.2) that:

1) a low reflective layer (10x) covers a portion of signal line (10), because the signal line (10) is manufactured of a metal film having relatively high reflectance, and another metal film (10x) having relatively low reflectance is formed on top of the first metal film.

2) Morita further discloses (col.4, lines 60-62; Fig.2) no black matrix between the upper substrate (60) and the pixel electrode (14) and above the low reflective layer, because the top substrate (60) is provided with no black mask aligned with the signal

lines (10), and the low reflective layer (10x) is formed on the signal line (10), so that the area does not have black layer also is above the low reflective layer (10x).

Morita indicates (col.4, lines 62 – 67) that to apply a relatively low reflective layer on the Al film so as to preclude unwanted light reflection. Because the low reflective layer shields the light to pass the signal line in stead of black matrix. For the same reason, using the low reflective layer to cover the gate line, the source area, drain area and channel region in stead of black matrix that would shield the light passing the gate line and the channel area, source area and drain area so as to preclude unwanted light reflection.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to modify the liquid crystal display of Morita such as Figs. 5-6 with the teachings of using low reflective layer on a metal layer and no black matrix between the top substrate and the pixel electrode as taught by Morita such as Fig.2 for precluding the unwanted light reflection, since such low reflective layer shielding unwanted light reflection (see col.4, lines 62 – 67).

Regarding claim 11, Morita discloses (col.5, lines 59 – col.6, line 65; Figs.5-6) that the passivation layer (planarization film 12 functions as passivation layer) formed over the gate line (gate electrode G connected to the gate line 43), the data line (the source electrode connected to the signal line 10), the low reflective layer (such as the low reflective layer 10x on the signal line 10); and the pixel electrode (14) formed on the passivation layer (12); and the pixel electrode (14) is connected to the TFT via a contact hole in the passivation layer (12).

Regarding claims 14 and 25, Morita discloses (col.7, lines 14-25; Fig.6) that a color filter (63) is formed on the color filter substrate (60); and liquid crystal (50) sealed between the color filter substrate (60) and transparent substrate (1).

4. Claims 3-4, 17, 19 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morita as applied to claims 1, 11, 14-15, 22 and 25 above, and further in view of US 6,172,728 (Hiraishi) and US 6,172,723 (Inoue et al).

Regarding claims 3-4, 17, 19 and 26, Morita further discloses (col.5, lines 59 – col.6, line 65; Figs.5-6) that the thin film transistor (TFT) includes:

- thin film transistor having gate electrode (G), source electrode (S)and drain electrode (D);
- gate electrode (G) connected to the gate line (43); and the gate electrode (G) being covered with the channel region (between the source area 7 and the drain area 8);
- source electrode is connected to the data line (signal line 10), drain electrode is connected to the pixel electrode (14); and drain electrode connected to the drain line that would an obvious variation as the source electrode connected to the data line for transferring data signal.

Morita teaches the invention set forth above. Morita lacks the low reflective layer formed on (or cover) the gate electrode or on the source and drain electrodes.

Hiraishi discloses (col.6, lines 34-37; Fig.1) that by providing a low-reflective film preferably made of chromium oxide (CrOx) on the gate lines (2) (the gate electrode is connected to the gate line) and the source lines (3) (data line) (the source electrode is

connected to the data line), the display quality is enhanced. Even though, the gate line and data line are not gate electrode or source/drain electrode, but forming a low reflective layer on the gate electrode and on the source/drain electrode that also is forming a low reflective layer on a metal layer that would be an obvious variation so as to enhancing the display quality.

As evidence, Inoue indicates (col.11, lines 34-50) that depositing a low reflection conductive material on a high reflection electrode (such as gate electrode, source electrode or drain electrode) so as to solver the problem in the art reducing the mixed reflected light (see col.1, lines 45-51). Therefore, those skilled in the art would be benefited from those teachings to form a low reflective layer patterned on an electrode such as the gate electrode and source/drain electrode to enhance the image display quality.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to modify the liquid crystal display of Morita with the teachings of forming a low reflective layer on the gate electrode, source electrode and drain electrode of the thin film transistor as taught by Hiraishi and Inoue for enhancing the image display quality, since low reflective layer shielding reflected light in the mixed light (see col.1, lines 45-51).

5. Claims 12-13 and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morita as applied to claims 1, 11, 14-15, 22 and 25 above, and further in view of US 6,172,728 (Hiraishi).

Regarding claims 12-13 and 23-24, Morita teaches the invention set forth above. Morita lacks that the pixel electrode is formed over (or overlap) a portion of the data line or a portion of gate line.

Hiraishi discloses (col.5, lines 56-57; Fig.1) that the pixel electrode (4) is formed over (or overlap) a portion of the data line (3) and a portion of the gate line (2), and the light leakage to the gap between the pixel electrodes and the gate lines or the date lines are prevented.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to modify the liquid crystal display of Morita with the teachings of the pixel electrode overlap a portion of data line or gate line as taught by Hiraishi, since the skilled in the art would be motivated for preventing the unnecessary leakage of light (see col.5, lines 56-57).

6. Claims 5-6 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morita as applied to claims 1, 11, 14-15, 22 and 25 above, and further in view of US 6,172,728 (Hiraishi) and Applicant admitted prior art (AAPA).

Regarding claims 5-6 and 20-21, Morita teaches the invention set forth above. Morita lacks that the low reflective layer is formed of CrOx, and the low reflective layer has a light reflectivity of 3% or less.

Hiraishi discloses (col.6, lines 34-37; Fig.1) that by providing a low-reflective film preferably made of chromium oxide (CrOx) on the gate lines (2) and the source lines (3) (data line), the display quality is enhanced.

Concerning the low reflective layer has a light reflectivity of 3% or less that is the property of the material (CrOx), and the same material must have the same property, and that would have been at least obvious.

As evidence, AAPA indicates (page 4, lines 2-3 of the specification) that the material of CrOx is widely used for black matrix to reduce the influences of the light reflection because the reflectivity of CrOx is about 3%. Therefore, the property of the CrOx (reflectivity is about 3%) must be widely known in the art. Widely used means "by or among a large well-dispersed group of people" (see Merriam-Webster's Collegiate Dictionary) utilized, and that should be common and known in the art.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to modify the liquid crystal display of Morita with the teachings of using chromium oxide as the material of the low-reflective film as taught by Hiraishi and AAPA for enhancing the display quality, since the material of chromium oxide having such low reflectance property (see col.6, lines 34-37).

Response to Arguments

7. Applicant's arguments filed on Aug.18, 2005 have been fully considered but they are not persuasive.

Applicant's arguments are as follows:

1) The references cannot be combined to reach the invention.

Examiner's responses to applicant's arguments are as follows:

1) The reference Morita is relied on a metal film having relatively high

reflectance, and another metal film (10x) having relatively low reflectance is formed on top of the first metal film; and there is no black matrix between the upper substrate (60) and the pixel electrode (14) in the Fig.2, i.e., an area between the pixel electrode (14) and the upper substrate (60), and above the low reflective layer (10x), is free of any black layer. Morita discloses an active-matrix display that is not limited to use backlight. Morita indicates (col.4, lines 62 – 67) that the top layer of the signal lines (10) of Al will cause its reflectance to be large enough to degrade the quality of image, such that a top layer of material having a relatively low reflectance is further applied on the Al film to preclude unwanted light reflection.

The reference Hiraishi is relied on providing a low-reflective film preferably made of chromium oxide (CrOx) on the gate lines (2) (the gate electrode is connected to the gate line) and the source lines (3) (data line) (the source electrode is connected to the data line), the display quality is enhanced. Even though, the gate line and data line are not gate electrode or source/drain electrode, but forming a low reflective layer on the gate electrode and on the source/drain electrode that also is forming a low reflective layer on a metal layer that would be an obvious variation so as to enhancing the display quality. Concerning the low reflective layer has a light reflectivity of 3% or less that is the property of the material (CrOx), and the same material must have the same property, and that would have been at least obvious.

The reference Inoue is relied on the evidence of depositing a low reflection conductive material on a high reflection electrode such as the gate electrode, source

electrode and drain electrode in order to solve the problem in the art and improve the image display quality.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Qi whose telephone number is (571) 272-2299. The examiner can normally be reached on M-T 8:00 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ROBERT KIM
SUPERVISORY PATENT EXAMINER

Mike Qi
September 15, 2005